Low Distortion RF-LDMOS Power Transistor for Wireless Communications Base Station Applications

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Abstract — **In this paper an LDMOS power transistor design is described having a square-law approximated transfer characteristic to obtain very low distortion in class-AB operation. Compared to conventional LDMOS transistors significant linearity improvement is achieved over a large power range. Measurements on a 30W/2GHz transistor demonstrates 5 to 10 dB improvement in intermodulation distortion (IMD) and single-carrier adjacent channel leakage ratio (ACLR) for WCDMA in the back-off region. The new LDMOS is very suitable for multi-carrier amplifiers in 3G system.**

I. Introduction

Base stations for existing and emerging standards for personal communication systems require cost effective RF power amplifiers. The new modulation formats which accommodate higher data rate services are designed to maximise spectral efficiency. RF power amplifiers are therefore challenged to amplify the complex modulated signals without distortion and at minimum dc power consumption. Low distortion and high efficiency are contradicting requirements for a power amplifier. A reasonable compromise is achieved with class-AB amplifiers. Currently, LDMOS is the technology of choice in this market, providing high gain and good linearity compared to other semiconductor technologies. However, the stringent linearity requirements for the complex modulation schemes, like EDGE-GSM and W-CDMA still require external linearization to meet the system specifications. Improved linearity on device level can help to reduce external linearization complexity and cost or increase output power level and efficiency.

In this paper an LDMOS device concept is described having a square law approximated transfer characteristic to obtain very low distortion in class-AB operation. The theory and design of this concept was already described in [1] and results obtained on device/circuit level was presented as well. This concept has now been utilized to improve LDMOS distortion on chip level by implementing this concept during wafer processing. The dominant distortion meachanism in LDMOS will reviewed first. Then the implementation will be discussed and finally results will presented at 2GHz for a 30W chip.

II. LDMOS Structure And Non-Linearity

A cross-section of the LDMOS structure used in this work is depicted in Fig. 1.

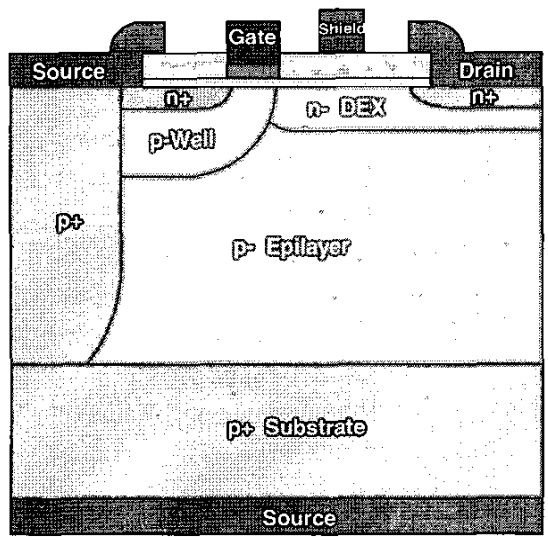

Fig 1. Cross-section of the LDMOS structure.

LDMOS devices have excellent RF capabilities due to a short channel, low feedback capacitance and low source inductance . The key part of the device from distortion point of view is the self-aligned channel formed by lateral diffusion of a p-type channel

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implant resulting in a non-uniform doping profile towards the drain end of the channel. This results in a non-linear current source $I_{ds}(V_{GS})$. Fig. 2 shows a typical transfer characteristic $I_{ds}=f(V_{GS})$ and transconductance g_m of a 30W LDMOS when biased in the saturated region (Vds= 10V). Several operating regions are identified in this picture with the following behaviour. In the sub-threshold region (A) the device exhibits an exponential behaviour. Above threshold, region (B), the device start to show a near square law type of behaviour and therefore linear g_m. This is typically the region for class-AB operation with low distortion. When the device enters region (C) velocity saturation sets in and the device shows a linear behaviour and therefore constant g_m. This is typically the region for class-A operation. In region (D) quasi-saturation effects sets in resulting from the lowly-doped drain drift region and the current starts to saturate resulting in a decrease of g_m.

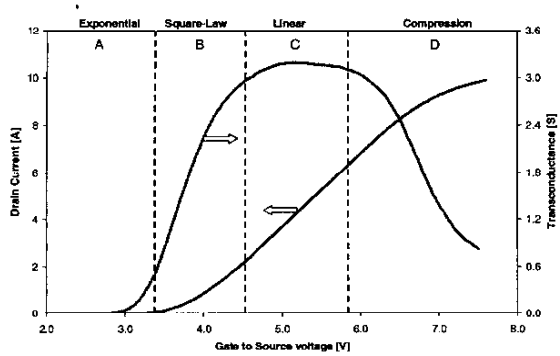

Fig. 2. LDMOS drain current and transconductance with 4 operating regions.

III. Distortion In Class-AB Operation

Linear amplifiers utilizing LDMOS transistors typically operate in class-AB since low distortion levels can be obtained with acceptable gain and efficiency. The IMD levels in the back-off region can be optimized with the gate bias voltage. It is well know that the odd-order derivatives of gm contribute to the odd-order IMD products [1]. The non-linear Id-Vgs relationship can be modeled by a Taylor series expansion around the bias point Vgs as follows [1]:

$$i_{ds}(t) = \sum_{k=1}^{\infty} \frac{1}{k!} \frac{d^k I_{DS}}{dV_{GS}^k}\bigg|_{V=V_{GS}} \cdot v_{gs}^k(t) = \sum_{k=1}^{\infty} g_{mk} \cdot v_{gs}^k \qquad (1)$$

were $v_{gs}(t)$ is a small-signal ac voltage around the bias point V_{GS}. Fig. 3 shows $I_D=f(V_{GS})$ and the first three odd-order Taylor coefficients of the conventional LDMOS in the region of interest.

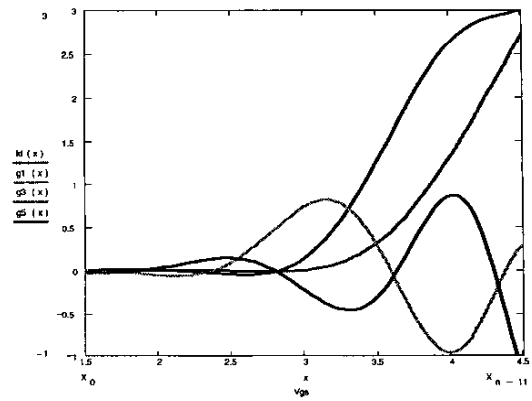

Fig 3. I_{DS} and Taylor coefficients g_{m1}, g_{m3} and g_{m5} versus Vgs of a conventional LDMOS.

For a two-tone signal the magnitude of IMD3 versus input voltage $V_{gs}(t)= V_S.(cos\varpi_1 t+cos\varpi_2 t)$ can be expressed as the ratio of the non-linear currents at the IMD frequency $ids,(2\varpi_1-\varpi_2)$ and fundamental frequency ids,ϖ_1 as follows [1]:

$$IMD_3 = \left| \frac{i_{ds,(2\omega_2-\omega_1)}}{i_{ds,\omega_1}} \right| = \left| \frac{\frac{3}{4} g_{m3} V_s^3 + \frac{25}{8} g_{m5} V_s^5}{g_{m1} V_s + \frac{9}{4} g_{m3} V_s^3 + \frac{25}{4} g_{m5} V_s^5} \right| \qquad (2)$$

From (2) it is evident that minimum IMD3 will be obtained if the device is biased in the region where g_{m3} and g_{m5} are zero. Since g_{m3} and g_{m5} have opposite signs the fifth-order term can compensate the third-order term and perfectly cancel (sweet spot) if these terms are also equal in magnitude. However, if distortion improvement is to be achieved over a wider power range the odd-order terms need to be minimized according to (2).

Fig. 4 shows the measured IMD3, 5 and 7 versus output power back-off (OPBO) for a conventional LDMOS at optimum gate bias level. When the ouput power is backed-off from te sweet-spot IMD3 starts to rise which, depending on the maximum level obtained, can prohibit the use of the device in e.g. multi-carrier applications. Also the level of IMD5 and 7 can restrict the use of the device if they exceed the

IMD3 level, e.g. near sweet spot. A preferred device should exhibit minimum level of IMD3 in the back-off region and IMD5 and IMD7 should not exceed this level.

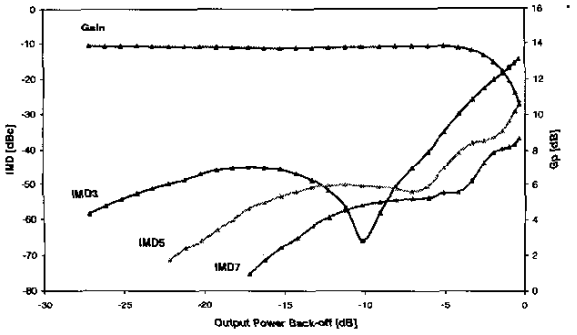

Fig 4. Two-tone distortion for a conventional class-AB LDMOS

Fig. 5 shows the single-tone gain (AM-AM) and phase (AM-PM) transfer characteristics versus drive power obtained with a network analyzer (NWA). Both have been normalized to the small-signal values. Both amplitude and phase distortion seems to contribute to the total istortion. Since IMD components generated from these two distortions types have a quadrature relation for memoryless PA, they add vectorially [2]. As will be shown later, the Taylor coefficients have more impact on amplitude distortion than on phase distortion.

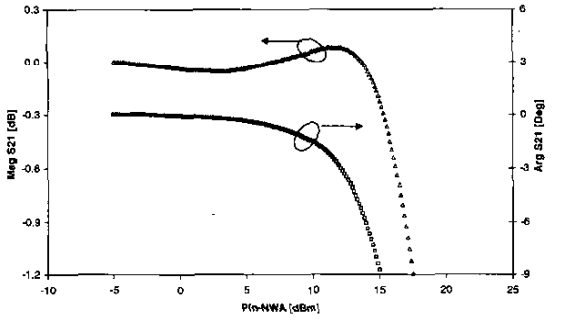

Fig 5. Normalised Gain (AM-AM) and Phase (AM-PM) transfer characteristics for a conventional class-AB LDMOS

III. Improved Distortion And Implementation

As argued in the previous section, lower distortion in the back-off region can be achieved if the odd-order Taylor coefficients are minimized in region B. The transfer characteristic $I_D=f(V_{GS})$ will then more closely approximate a square-law behavior. A well known technique to shape the transfer characteristic is the Derivative Superposition (DS) method described in [3]. In [1] this concept was applied on a 5W level utilizing four paralleled discrete LDMOS devices of different sizes each externally biased at different V_{GS} levels such that g_{m3} , g_{m5}, etc. were minimized. A disadvantage of this implementation form is the increased complexity in bias circuitry. In addition re-optimization of size and V_{GS} is required if the power is scaled.

An implementation form that circumvents these problems is a discrete LDMOS chip with distributed *Vth*. A conventional discrete LDMOS chip comprises a number of paralleled FETs in an interdigitated finger structure with uniform *Vth*. In the new LDMOS structure the active area is divided into *n* parallel sections each having different *Vth* and channel width *(Wg)*. This set of parameters is used to optimize $I_D=f(V_{GS})$ to achieve a better square law behaviour in region (B) of fig. 2. This results in a very cost effective implementation of this concept through chip layout design, *n* and *Wg*, and a few additional processing steps to define the *Vth*. In order to obtain a scalable structure, small unit FETs with distributed Vth are defined that can been paralleled to obtain higher power output.

Fig. 6 shows $I_D=f(V_{GS})$ and g_{m1}, g_{m3} and g_{m5} of the new 30W LDMOS with distributed *Vth* using a 3-section approach. The *Vth* of these 3 paralleled FETs have a symmetrical offset and their *Wg* are unequal in size. Compared to fig. 3 a significant reduction has been obtained in g_{m3} and g_{m5} without sacrificing g_{m1}. Also there is more symmetry in g_{m3} and g_{m5} which accommodates distortion compensation over a larger signal range.

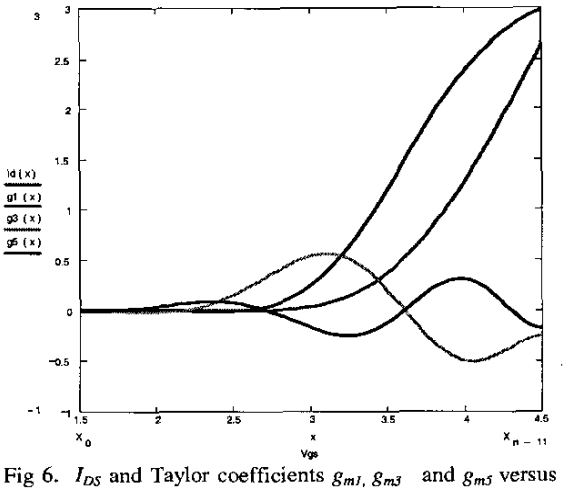

Fig 6. I_{DS} and Taylor coefficients g_{m1}, g_{m3} and g_{m5} versus Vgs of the improved LDMOS.

IV. Performance Of The New LDMOS

Fig. 5 shows the gain and phase transfer characteristics of the distributed *Vth* and conventional LDMOS. It is clear from this picture that the gain shape in back-off is affected significantly by g_m profiling while the shape of the phase is hardly affected.

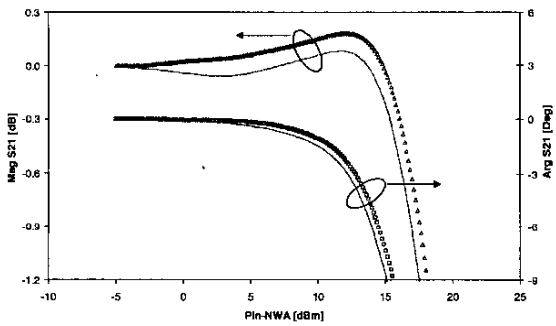

Fig 7. Normalised Gain (AM-AM) and Phase (AM-PM) transfer characteristics for the new (markers) and conventional (line) class-AB LDMOS

Fig. 8 shows IMD3, 5 and 7 of the distributed *Vth* and conventional LDMOS versus output power back-off. A significant reduction in distortion is obtained in the back-off region for all IMDs. The overall distortion improvement commences at about 8dB back-off where IMD3 of the new design equals IMD5 of the conventional design. At 10dB back-off the overall improvement is about 5dB and increases up to 10dB and more if the power is backed-off further.

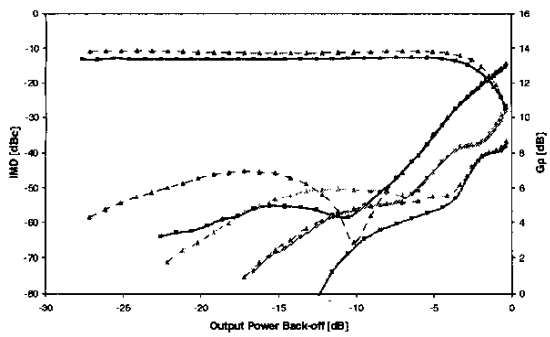

Fig 8. IMD3, 5 and 7 of the conventional (dashed lines) and improved LDMOST(solid lines)

Fig. 9 shows ACLR for a single carrier 3GPP-WCDMA signal for the distributed *Vth* and conventional LDMOS versus output power back-off. ACLR5 improvement commences at 9dB back-off and reaches maximum improvement of about 7dB at 14dB back-off.

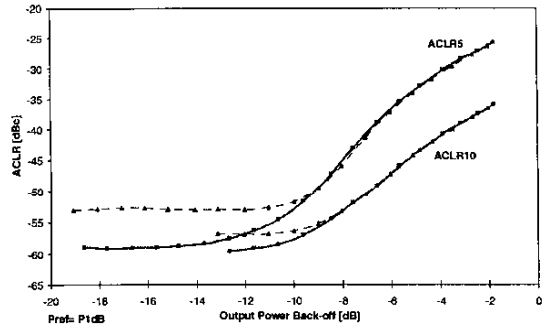

Fig 9. ACLR of the conventional (dashed line) and improved LDMOST(solid line)

IV. Conclusions

An new LDMOS transistor has been presented with improved distortion characteristics utilizing a distributed Vth concept. The distortion improvement in the back-off region is 5 to 10dB for two-tone IMD. For a single carrier 3GPP-WCDMA signal up to 7dB improvement is obtained in the back-off region. The new LDMOS transistor can therefore help to reduce linearization complexity and cost or to increase ouput power level and efficiency.

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